UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/693,358	10/19/2000	Coke S. Reed	M-9051 US	8267

32794 7590 06/23/2004

KOESTNER BERTANI LLP
18662 MACARTHUR BLVD
SUITE 400
IRVINE, CA 92612

EXAMINER	
JUNTIMA, NITTAYA	

ART UNIT	PAPER NUMBER
2663	10

DATE MAILED: 06/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/693,358	REED ET AL.	
	Examiner	Art Unit	
	Nittaya Juntima	2663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-39,43-50 and 52-55* is/are allowed.

6)☒ Claim(s) *40-42,51 and 56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 October 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the amendment filed on February 9, 2004.

2. The objection to the specification and the rejections under 35 U.S.C. 112, second paragraph to claims 3, 11-14, 27, 29, 37, and 39-40 are withdrawn in view of applicant's amendment.

3. Claims 1-39, 43-50, and 52-55 are allowed.

4. Claims 40-42 and 51 are presently rejected under 35 U.S.C. 102 (b).

5. Claim 56 is rejected under 35 U.S.C. 103 (a).

Specification

6. The disclosure is objected to because of the following informalities:

- the U.S. patent application number (09/693,???) on pg. 16, ll 27-29 and pg. 17, ll 10-12 should be updated.

Appropriate correction is required.

Claim Objections

7. Claims 1, 3, 37, and 40-43 are objected to because of the following informalities:

- in claim 1, ll 16, "manage" should be changed to "manages;"
- in claim 3, ll 5, "exists" should be deleted; and

  ll 6, "D" should be changed to "B;"
- in claim 37, ll 13, "a group" should be changed to "the group;"

- in claim 40, ll 20, "connections" should be changed to "interconnections;"

- in claim 41, ll 14-17, "the message M" should be changed to "the messages M," see ll 13 of the claim,

ll 19-34, "the message M" should be changed to "each of the messages M;"

ll 35, "message M" should be changed to "message's;

- in claim 42, ll 13, ""of" should be deleted;

- in claim 43, ll 25, "B1," "B2," and "and/or" should be changed to "D1," "D2," and "or," respectively.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. **Claims 40-42** and **51** are rejected under 35 U.S.C. 102(b) as being anticipated by an art of record, Coke S. Reed (WO 97/04399).

Per **claim 40**, Reed teaches a network capable of carrying ***a plurality of messages M concurrently*** (more than one message data is being carried in the network, page 5, lines 1-3), ***the messages including high QoS messages*** (ATM cells with CBR QoS) ***and low QoS messages*** (e.g. ATM cells with UBR QoS) (it is inherent that messages M must include ATM cells with

different QoS, i.e. CBR and UBR, when ATM machines are used in the network, page 4, lines 13-18), ***a plurality of output ports P*** (output ports of devices connected to but reside outside the interconnect structure, i.e. devices E and F, page 5, lines 3-7), ***a plurality of nodes N*** (page 4, lines 21-27), ***the individual nodes N including a plurality of direct message input interconnections and a plurality of direct message output interconnections*** (page 4, lines 28-page 5, lines 1, and page 17, lines 8-20 and Fig. 3B), ***the individual nodes N for passing messages M to predetermined output ports*** (designated output ports of destination devices) ***of the plurality of output ports P and the predetermined output ports P being designated by the messages M*** (page31, lines 25-page 32, lines 1-2 and page 4, lines 27-28), ***a plurality of interconnect lines in an interconnect structure selectively coupling the nodes in a hierarchical multiple level structure arranged to include a plurality of J+1*** (J+1) ***levels in an hierarchy of levels arranged from a lowest destination level L_0 to a highest level L_J which is farthest from the lowest destination level L_0*** (page 4, lines 21-27 and page 5, lines 19-20), ***the output ports P being connected to nodes at the lowest destination level L_0*** (output ports of destination devices are connected to nodes on a level zero, page 4, lines 27-28 and page 5, lines 3-6, see also page 31, lines 25-page 32, lines 1-2), ***the level of a node being determined entirely by its position in the structure*** (page 6, lines 24-27, and page 7, lines 21-page 8, lines 1-7), ***the network includes a node A*** (node E in Fig. 3B), ***a control signal operating to limit the number of messages that is allowed to be sent to the node A*** (node E in Fig. 3B) ***to eliminate contention for the predetermined output ports of the node A*** (in Fig. 3B, node F sends a control signal to node A to indicate a blocking as node F sends message to node E, page 7, lines 1-8, 15-20, and page 10, lines 14-19, see also page 30, lines 14-21) ***so that the messages M are sent through the direct***

message output interconnections of the node A to nodes H (nodes H read on nodes at lower level on the path toward the destination level 0, page 10, lines 14-19) ***that are a level L no higher than the level of the node A, the nodes H being on a path to the designated predetermined output ports P of the messages M*** (page 9, lines 21-26, page 22, lines 11-18, and page 31, lines 25-page 32, lines 1-2), ***the control signal is being determined at least partly according to message quality of service*** (priority) ***and position of the node A*** (in Fig. 3B, node F located on the same level T-1 as node E having higher priority message sends control information to node A on the adjacent outer level T to warn of impending conflicts, page 7, lines 8 and 15-20, page 10, lines 16-22, page 30, lines 14-21, and page 47, lines 3-6).

Per **claim 41**, Reed teaches an interconnect apparatus comprising a plurality of nodes and a plurality of interconnect lines (page 4, lines 21-24), a plurality of J+1 levels in an hierarchy of levels arranged from a lowest destination level L_0 to a highest level L_J (page 24, lines 24-28 and page 5, lines 19-20), the level of a node (node A in Fig. 3B) being determined entirely by its position (page 9, lines 1-5), the interconnect structure transmitting a plurality of multiple-bit messages entering the interconnect structure unsorted through a plurality of input ports (input ports of nodes at level J) (page 5, line 10, page 22, lines 11-12, 15-18, page 31, lines 25-page 32, lines 1-2), individual messages M being self-routing (having header designating the target ring in a binary form, page 31, lines 25-page 32, lines 1-2) and including high QoS messages (ATM cells with CBR QoS) and low QoS messages (e.g. ATM cells with UBR QoS) (it is inherent that messages M must include ATM cells with different QoS, i.e. CBR and UBR, when ATM machines are used in the network, page 4, lines 13-18), ***movement of each of the messages M being determined by quality of service*** (priority level) ***of each of the messages M and the node***

(node A in Fig. 3B) ***position*** (in Fig. 3B, message M from node A having lower priority than message from node F moves from node A to node E on a lower level or to another node on the same level depending whether a control code is sent to node A from node F, page 7, lines 8 and 15-20, page 9, lines 21-26, page 10, lines 16-22, page 30, lines 14-21, and page 47, lines 1-6), ***each of the messages M exits an output port designated by each of the messages M*** (page 31, lines 25-page 32, lines 1-2) ***using the three ways being (1) each of the messages M enters a node*** (node N (J,θ_1,z_1)) ***in the interconnect structure from an external device*** (CU (θ_1,z_1)) (page 32, lines 24-26), ***each of the messages M designating one designated output port*** (CU(θ_2,z_2)) (page 31, lines 25-page 32, lines 1-2), ***(2) each of the messages M moves through a node*** (node N(T,θ, z)) ***to a designated output port*** (CU(θ_2,z_2)), ***a time T being associated with the node such that each of the messages M arriving at the node is selectively transmitted within the time T of the message's arrival at the node*** (page 31, lines 22-page 33, lines 1-5), ***(3) the message M moves either (i) through a node U*** (node N(r,θ, z) = N(T,θ, z)) ***on a level L_k*** (level r, where r = T) ***to a different node V*** (node N($T,\theta+1,h_T(z)$) ***on the same level L_k in combination with another message, if available, or (ii) moves through the node U on a level L_k to a node W*** (node N(T-1, θ+1,z)) ***on a level L_i*** (T-1) ***nearer in the hierarchy to the destination level L_0 than the level L_k*** (page 33, lines 6-26), ***a time T_U being associated with the node U such that the message M arriving at the node U is selectively transmitted within the time TU of the message M arrival at the node U*** (page 31, lines 22-25, page 32, lines 3-22, and page 33, lines 6-26).

Per **claim 42**, Reed teaches an interconnect structure comprising ***a plurality of nodes and a plurality of interconnect lines*** (page 4, lines 21-24), ***the interconnect structure transmitting a plurality of multiple-bit messages entering the interconnect structure unsorted through a***

plurality of input ports (input ports of nodes at level J) (page 5, line 10, page 22, lines 11-12, 15-18, page 31, lines 25-page 32, lines 1-2), ***an individual message M being self-routing*** (having a header designating the target ring in a binary form, page 31, lines 25-page 32, lines 1-2), ***the interconnect structure includes a node E*** (node E in Fig. 3B) ***having a first data input interconnection from a node A*** (node A in Fig. 3B) ***and a second data input interconnection from a node F*** (node F in Fig. 3B) ***distinct from the node A, and a control interconnection*** (a dotted line from F to A in Fig. 3B) ***between the node A and node F for carrying a control signal to resolve contention for sending messages to the node E*** (page 7, lines 1-20 and page 17, line 15), ***the control signal resolving contention at least partly on the basis of QoS*** (the basis of QoS is not defined, therefore, translates into priority of message where a message from node F on the same level as node E has higher priority than a message from node A located one level above node E, page 7, lines 15-20 and page 47, lines 3-6) and ***position in the structure of the node A*** (in Fig. 3B, control information is sent from node F on level T-1 to node A on the adjacent outer level T to warn of impending conflicts, page 7, lines 18-20, page 17, line 15, and page 47, lines 3-6).

Per **claim 51**, as shown in Fig. 3B, Reed teaches an interconnect structure comprising ***a collection of nodes including distinct nodes A*** (A), ***B*** (D), ***C*** (F), and ***D*** (E) (page 4, lines 21-24), ***a collection of interconnect lines selectively coupling the nodes of the interconnect structure*** (page 4, lines 21-24, page 17, lines 8-20, and Fig. 3B), ***a logic*** (switch logic) ***for routing packets through the interconnect structure so that the node A*** (A) ***is capable of sending packets to the node B*** (D) ***or the node D*** (E) (page 33, lines 6-26), ***for a packet PA arriving at the node A and a packet PC*** (message m_1) ***arriving at the node C*** (F), ***the node C***

has routing priority over the node A to send messages to the node D (E) ***in which routing of the packet PA*** (message M) ***at the node A*** (A) ***depends upon routing of the packet PC*** (message m_1) ***at the node C*** (F) (page 29, lines 25-28, page 30, lines 14-21, and page 47, lines 3-6), and ***routing of the packet PC*** (message m_1) ***at the node C*** (F) ***depends at least partly on a QoS of service of the packet PC*** (message m_1) ***and position in the interconnect structure of the node A*** (A) (node F located on the same level as node E has message with top priority, whereas a message from node A of lower level has second priority, page 7, lines 8 and 15-20, page 10, lines 16-22, page 30, lines 14-21, and page 47, lines 3-6).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. **Claim 56** is rejected under 35 U.S.C. 103(a) as being unpatentable by an art of record, Coke S. Reed (WO 97/04399).

Per **claim 56**, as shown in Fig. 3B, Reed teaches an interconnect structure comprising ***a plurality of nodes*** (page 4, lines 21-24) ***including the distinct nodes A*** (A), ***B*** (D), ***C*** (F), ***and D*** (E) (page 4, lines 21-24), ***a collection of interconnect lines selectively coupling the nodes of the interconnect structure*** (page 4, lines 21-24, page 17, lines 8-20, and Fig. 3B), ***including one data carrying line allowing the node A to send messages to the node B, one data carrying line allowing the node A*** (A) ***to send data to the node D*** (E), ***and one data carrying line allowing***

for the node C (F) ***to send data to the node D*** (E) (page 17, lines 8-20), and ***a logic*** (switch logic) ***for routing packets through the interconnect structure so that a message M_C*** (message m_1) ***arriving at the node C*** (F) ***is not blocked from being routed to the node D*****(E)** ***by a message M_A*** (message M) ***arriving at the node A*** (A) (page 33, lines 6-26, page 29, lines 25-28, page 30, lines 14-21, and page 47, lines 3-6), ***messages arriving at the node A*** (A) ***are routed by a logic associated with the node A*** (A) ***to other nodes in the interconnect structure*** (page 33, lines 6-26), ***the logic*** (logic switch) ***at node A*** (A) uses position of the node A (A) in the structure in part to route the messages arriving at node A (A) to other nodes (D and E) in the interconnect structure (page 9, lines 21-26, page 30, lines 14-21 and page 47, lines 3-6)

Reed fails to teach that the logic at node A also use QoS information from the messages arriving at node A to route the messages arriving at node A to other nodes in the interconnect structure.

However, Reed also teaches that ATM machines are used in the interconnect structure (page 4, lines 16-18), therefore, messages must be ATM cells with different QoS levels, e.g. CBR with high QoS or UBR with low QoS as known in the art.

Therefore, it would have been obvious to one skilled in the art to modify the logic at node A such that the logic would also use QoS information (e.g. CBR and UBR) from the messages arriving at node A at least in part to route the messages to other nodes in the structure. The motivation/suggestion to do so would have been to ensure the QoS of the messages such that messages with CBR would have priority over messages with UBR.

Response to Arguments

12. Applicant's arguments with respect to claims XXX have been fully considered but they are not persuasive.

a) In the remarks regarding claims 40-42 and 51, the applicant argues that the claims have been further clarified the novel usage of quality-of-service by including the position of the node A in the structure and therefore are now allowable.

In response, Reed teaches that (i) control information is sent from nodes on a level to nodes on the adjacent outer level to warn of impending conflicts (page 7, lines 18-20), (ii) the message one level toward the destination level of the third dimension when the en route node is not blocked and moving the message in the first and second dimensions along a constant level in the third dimension otherwise (page 9, lines 20-26 and page 30, lines 14-21), and (iii) a message on the same level has top priority (quality of service) and a message from a node one level above has second priority (page 47, lines 3-6). Therefore, Reed explicitly teaches determining the control signal, movement of the message, and resolving contention using the control signal at least in part according the message quality of service and position of the node A (node A in Fig. 3B) as recited in claims 40-42 and 51. The rejection is maintained.

b) In the remarks regarding claim 56, the applicant argues that the claim has also been further clarified the novel usage of quality-of-service by including the position of the node A in the structure and therefore is now allowable.

In response, Reed teaches that (i) control information is sent from nodes on a level to nodes on the adjacent outer level to warn of impending conflicts (page 7, lines 18-20), (ii) the message one level toward the destination level of the third dimension when the en route node is not blocked and moving the message in the first and second dimensions along a constant level in

the third dimension otherwise (page 9, lines 20-26 and page 30, lines 14-21), and (iii) a message on the same level has top priority (quality of service) and a message from a node one level above has second priority (page 47, lines 3-6). Therefore, Reed explicitly teaches determining the control signal and movement of the message and resolving contention using the control signal at least in part according the message quality of service and position of the node A (node A in Fig. 3B) as recited in the claim.

Although Reed fails to teach that the logic at node A also use QoS information from the messages arriving at node A to route the messages arriving at node A to other nodes in the interconnect structure, Reed fruther teaches that ATM machines are used in the interconnect structure (page 4, lines 16-18), therefore, messages must be ATM cells with different QoS levels, e.g. CBR with high QoS or UBR with low QoS as known in the art.

Therefore, it would have been obvious to one skilled in the art to modify the logic at node A such that the logic would also use QoS information (e.g. CBR and UBR) from the messages arriving at node A at least in part to route the messages to other nodes in the structure. The motivation/suggestion to do so would have been to ensure the QoS of the messages such that messages with CBR would have priority over messages with UBR. The rejection is maintained.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nittaya Juntima whose telephone number is 703-306-4821. The examiner can normally be reached on Monday through Friday, 8:00 A.M - 5:00 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chau Nguyen can be reached on 703-308-5340. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nittaya Juntima
June 15, 2004
NJ

CHAU NGUYEN
PATENT EXAMINER